Amendments to the Claims:

The following listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A data transfer control device for transferring data between a plurality of nodes connected to a bus, the data transfer control device comprising:

a circuit which generates identification information for determining whether or not one received packet and a next received packet are received during different reset intervals, when a reset interval is defined as the period between a reset that clears node topology information and the next reset;

a write circuit which links each received packet with the generated identification information, and writes the received packet and identification information into a packet storage memory; ~~and~~

a first pointer storage register which stores first pointer information that specifies a boundary in the packet storage memory between an area for a packet received before the occurrence of a reset that clears node topology information and an area for a packet received after the occurrence of the reset~~.~~;

wherein the identification information is a toggle bit that toggles from zero to one or from one to zero when one received packet and the next received packet are packets received within different reset intervals; and

wherein the identification information for the one received packet is different than the identification for the next received packet.

2. (Canceled).

3. (Previously Presented) The data transfer control device as defined in claim 1,

wherein the packet storage memory is a randomly accessible storage memory and is divided into a control information area in which is stored packet control information and a data area in which is stored packet data; and

wherein the identification information is included within the control information written to the control information area.

4. (Canceled).

5. (Currently Amended) The data transfer control device as defined in ~~claim~~ 4claim 1,

wherein a start address of the next packet after a packet that was received immediately before the occurrence of a reset is stored as the first pointer information in the first pointer storage register.

6. (Currently Amended) The data transfer control device as defined in ~~claim~~ 4claim 1, further comprising:

a second pointer storage register which stores second pointer information which specifies a boundary in the packet storage memory between an area for processed packets and an area for unprocessed packets; and

a third pointer storage register which stores third pointer information which specifies a boundary in the packet storage memory between an area for received packets and an area storing no received packets.

7. (Currently Amended) The data transfer control device as defined in ~~claim~~ 4claim 1, further comprising:

a processing unit which specifies a packet received after the occurrence of the reset, based on the first pointer information stored in the first pointer storage register, and gives priority to processing the specified packet.

8. (Currently Amended) The data transfer control device as defined in ~~claim 4~~claim 1,

wherein the packet storage memory is a randomly accessible storage memory and is divided into a control information area in which is stored packet control information and a data area in which is stored packet data; and

wherein the first pointer storage register includes:

a fourth pointer storage register which stores fourth pointer information which specifies a boundary in the control information area between control information for a packet received before the occurrence of the reset that clears node topology information and control information for a packet received after the occurrence of the reset; and

a fifth pointer storage register which stores fifth pointer information which specifies a boundary in the data area between data of a packet received before the occurrence of the reset that clears node topology information and data of a packet received after the occurrence of the reset.

9. (Original) The data transfer control device as defined in claim 8,

wherein the data area has been divided into a first data area for storing first data for a first layer and a second data area for storing second data for a second layer; and

wherein the fifth pointer information is pointer information which specifies a boundary in the first data area between the first data for a packet received before the occurrence of the reset that clears node topology information and the first data for a packet received after the occurrence of the reset.

10. (Currently Amended) ~~A~~ The data transfer control device ~~for transferring data between a plurality of nodes connected to a bus, the data transfer control device~~as defined in claim 1, comprising:

~~a read circuit which reads a packet from a packet storage memory when a transmission start command has been issued;~~

~~a link circuit which provides services for transmitting read packet to each node;~~

a status storage register which stores status information indicating that the transmission of a packet has been halted, when the transmission of the packet has been halted by the occurrence of a reset that clears node topology information~~; and~~

~~a first pointer storage register which stores first pointer information that specifies a boundary in the packet storage memory between an area for a packet received before the occurrence of a reset that clears node topology information and an area for a packet received after the occurrence of the reset.~~.

11. (Previously Presented) The data transfer control device as defined in claim 10, further comprising a processing unit which issues the transmission start command;

wherein the processing unit cancels transmission processing that has already started, without determining whether or not transmission has been completed, when it has been determined from the status information that transmission of a packet has been halted by the occurrence of the reset.

12. (Original) The data transfer control device as defined in claim 1,

wherein the reset is a bus reset as defined by the IEEE 1394 standard.

13-17. (Canceled).

18. (Previously Presented) Electronic equipment comprising:

a data transfer control device as defined in claim 1;

a device which performs given processing on data that has been received from another node through the data transfer control device and a bus; and

a device which outputs or stores data that has been subjected to processing.

19-20. (Canceled).

21. (Previously Presented) Electronic equipment comprising:

a data transfer control device as defined in claim 1;

a device which performs given processing on data that is to be transferred to another node through the data transfer control device and a bus; and

a device which takes in data to be subjected to processing.

22-23. (Canceled).

24. (Currently Amended) A data transfer control device for transferring data between a plurality of nodes connected to a bus, the data transfer control device comprising:

a circuit which generates identification information for determining whether or not one received packet and a next received packet are received during different reset intervals, when a reset interval is defined as the period between a reset that clears node topology information and the next reset;

a write circuit which links each received packet with the generated identification information, and writes the received packet and identification information into a packet storage memory; ~~and~~

wherein a changing point of the identification information specifies a boundary in the packet storage memory between an area for a packet received before the occurrence of a reset that clears node topology information and an area for a packet received after the occurrence of the reset~~.~~;

wherein the identification information is a toggle bit that toggles from zero to one or from one to zero when one received packet and the next received packet are packets received within different reset intervals; and

wherein the identification information for the one received packet is different than the identification for the next received packet.

25. (Previously Presented) The data transfer control device as defined in claim 24,

wherein the packet storage memory is a randomly accessible storage memory and is divided into a control information area in which is stored packet control information and a data area in which is stored packet data; and

wherein the identification information is included within the control information written to the control information area.